[source/drain] regions 34, the [latter] source/drain pockets 32 adjoining the channel region 24. Alternatively, a deeper [source/drain] implant may be performed to extend [source/drain] regions 34 over the bottom portions of source/drain pockets 32. Either one of these well-known methods reduces the capacitance of the transistor, thereby improving transistor performance."

In the claims:

Amend claim 1 as follows:

1. (Four Times Amended) A field effect transistor comprising:

a region of semiconductor material doped a first conductivity type;

a source of said first conductivity type and a drain of said first conductivity type, both said source and said drain disposed in said region of semiconductor material and a counterdoped region of opposite conductivity type disposed within said source and within said drain and [separated by] isolated from the remaining portion of said region of semiconductor material by said source and drain;

a counterdoped channel region disposed in said region of semiconductor material between said source and said drain;

said counterdoped channel region having a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region being the primary conduction channel of said transistor and having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source and said drain.

Referring to FIGURE 1E, n-type regions 34 are formed within p-type source/drain pockets 32 using ion implantation. In this example, regions 34 are implanted with an n-type material such as arsenic.. Although source/drain pockets 32 are shown extending around regions 34 and adjoining isolation trenches 20, it will be understood that source/drain pockets 32 may extend only along the inside portion of regions 34, the source/drain pockets 32 adjoining the channel region 24. Alternatively, a deeper implant may be performed to extend regions 34 over the bottom portions of source/drain pockets 32. Either one of these well-known methods reduces the capacitance of the transistor, thereby improving transistor performance.

1. A field effect transistor comprising:

a region of semiconductor material doped a first conductivity type;

a source of said first conductivity type and a drain of said first conductivity type, both said source and said drain disposed in said region of semiconductor material and a counterdoped region of opposite conductivity type disposed within said source and within said drain and isolated from the remaining portion of said region of semiconductor material by said source and drain;

a counterdoped channel region disposed in said region of semiconductor material between said source and said drain;

said counterdoped channel region having a first region of one of undoped or doped opposite conductivity type and a second doped region underlying the first region of said opposite conductivity type, said second doped region being the primary conduction channel of said transistor and having a greater charge-carrier mobility than said first region, said second doped region being the primary conduction channel between said source and said drain.